CGC

Docket No. CISCO-4330 (032590-000158)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Srinivasaiah et al.

SERIAL NO.: 09/909,658

FILING DATE: July 19, 2001

TITLE: BOUNDARY SCAN CELL FOR TESTING AC COUPLED LINE USING PHASE MODULATION TECHNIQUE

PATENT NO.: 6,877,121

ISSUED: April 5, 2005

EXAMINER: Albert DeCady (Primary) and Esaw Abraham (Assistant)

ART UNIT: 2133

CERTIFICATE OF MAILING

I hereby certify that this paper is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450, on the date printed below:

Date: August 2, 2005 Name: P Sherman
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TRANSMITTAL FOR CERTIFICATE OF CORRECTION

We enclose, pursuant to the provisions of 37 C.F.R. §1.322, a Certificate of Correction for United States Patent No. 6,877,121. Please make the Certificate of Correction and the statements herein of record.

The corrections made to the above-identified United States Patent in the Certificate of Correction filed herewith are to correct mistakes which are of a minor character according to 35 U.S.C. §254 and 37 C.F.R. §1.322. The proposed corrections do not

constitute such changes in the patent as would constitute new matter or would require re-examination.

37 C.F.R. §1.322 Corrections

Please see attached Certificate of Correction.

No Fee Due

It is believed that no fee is required for filing the above-noted document. In the event any fee is required for filing of this Certificate of Correction, the Assistant Commissioner is hereby authorized to charge the fee to our Deposit Account No. 50-1698.

Respectfully submitted,
THELEN REID & PRIEST LLP

Dated: August 2, 2005

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UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO : 6,877,121

DATED : April 5, 2005

INVENTOR(S) : Srinivasaiah et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

1) In section 57 of the cover page after receiving IC then compares the phase of, replace "a source of" with --the--.

2) In section 57 of the cover page after phase captured at the, replace "snyc" with --sync--.

3) In column 3 line 11, replace "VO" with --I/O--.

4) In column 6 line 7, replace "bscanshiftIn" with --bscanShiftIn--.

5) In column 6 line 12, replace "BSCS" with --BSCs.--.

6) In column 8 line 9, replace "Rate" with --gate--.

7) In column 9 line 29 replace "expect" with --except--.

8) In column 9 line 54 after AC, insert --signal--.

9) In column 9 line 56, replace "method-according" with --method according--.

10) In column 13 line 3 replace "refclk" with --refClk--.

11) In column 13 line 12 replace "Rate" with --gate--.

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PATENT NO. 6,877,121

No. of additional copies

⇨ 1

Serial/Patent.No.: [not yet assigned] Filing/Issue Date: 7/[illegible]2001

Client: Cisco

Title: Boundary Scan Cell for Testing AC Coupled Line Using Phase Modulation Technique

jc978 U.S. PTO 09/909658

TRP File No.: CISCO-4330 Atty/Secty Initials: TL/dm

Date Mailed: 7/19/01 Docket Due Date: 07/19/01

The following has been received in the U.S. Patent & Trademark Office on the date stamped hereon:

- ☐ Amendment/Response (_____ pgs.)
- ☐ Appeal Brief (_____ pgs.) (in triplicate)
- ☒ Application - Utility (30 pgs. with cover & abstract)
- ☐ _____ Pieces of Prior Art Enclosed
- ☐ Application – Rule 1.53(b) Continuation (_____ pgs.)
- ☐ Application – Rule 1.53(b) Division (_____ pgs.)
- ☐ Application – Rule 1.53(b) CIP (_____ pgs.)
- ☐ Application – Rule 1.53(d) CPA (_____ pgs.)
- ☐ Application – Design (_____ pgs.)
- ☒ Drawings: 10 # of sheets includes 12 figures 30153
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- ☐ Issue Fee Transmittal ☐ Deposit Acct. No. #
- ☐ Notice of Appeal Amt:
- ☐ Petition for Extension of Time
- ☐ Petition for

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- ☐ Application – Rule 1.53(d) CPA (_____ pgs.)
- ☐ Application – Design (_____ pgs.)
- ☐ Application – PCT (_____ pgs.)
- ☐ Application – Provisional (_____ pgs.)
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Client/Matter # 32590 - 158

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ABSTRACT OF THE DISCLOSURE

An apparatus and a method for testing Alternating Current (AC) coupled interconnects of a circuit using boundary scan methodology are disclosed. A Boundary Scan Cell (BSC) of a transmitting Integrated Circuit (IC) generates an AC signal based on a value of the BSC of the transmitting IC and a reference clock. A Sync Pulse cell at the receiving IC generates a sync pulse signal to the BSC of the receiving IC. The BSC of the receiving IC captures a default phase of the AC signal in relation to the sync pulse signal and also captures a phase of a source of input signal. The BSC of the receiving IC then compares the phase of the input signal with the phase of said AC signal in relation to the phase captured at the sync pulse signal and sends out an output signal based on the comparison.

output structure, a BSC is inserted between the system control signal output line of the core logic and the bi-directional output buffer. Also, a bi-directional BSC is inserted between the core logic and the bi-directional output buffer.

[0009] Turning first to FIG. 1, a detailed logic block diagram of a prior art BSC 10 is shown. The BSC 10 includes a boundary scan mode multiplexer (mode multiplexer) 12, a shift multiplexer 14, a data shift/capture register 16, and an update data register 18. The mode multiplexer 12 and the shift multiplexer 14 each have a system input (0), an update input (1), an output, and a select line. The data shift/capture register 16 and the update data register 18 each have a data input (D), a clock input (CLK), a normal output (Q), and an inverted output (Q bar or not Q).

[0010] The BSC 10 includes a system data input (SDI) line for receiving system signals including system data signals and system control signals from the system signal output lines, including the system data signal output lines and the system control signal output lines, of the core logic. If the BSC 10 is used for control purposes, the SDI line may receive a system control signal from the core logic. If the BSC 10 is used for output, the SDI line may receive a system data signal from the core logic. If the BSC 10 is used for an input, the SDI line becomes a system data received input (SDRI) line for receiving signals from the I/O pin through an input buffer. The BSC 10 also includes a system data output (SDO) line for transmitting signals through an output buffer to the I/O pin. If the BSC 10 is used for an input, the SDO line becomes a system data received output (SDRO) line for transmitting signals to the core logic. The SDI line and the SDO line

Correction 3

invention. A first net 402 has a missing capacitor in its circuit. A second net 404 has an opening in its circuit on the driving end. A third net 406 has an opening in its circuit on the receiving end. A fourth net 408 has a driving end stuck at 0. A fifth net 410 has a driving end stuck at 1. A sixth net 412 has a receiving end stuck at 0. A seventh net 414 has a receiving end stuck at 1.

[0035] FIG. 5 is a block diagram illustrating a transmitting boundary scan cell (BSC) according to a specific embodiment of the present invention. The circuit 502 in the box with broken lines represents a transmitter BSC according to a specific embodiment of the present invention. Such transmitter BSC is capable of acting as an ordinary boundary scan cell as well as handling AC signals.

[0036] The transmitter BSC comprises a shift/capture flip-flop 504, an update flip-flop 506, an XOR logic gate 508, and a multiplexor 510. The shift flip-flop 504 is connected to three sources of signals or data input: *bscanShiftIn*, *clockBscanAc*, and *testBscanReset*. The *bscanShiftIn* line allows AC test stimulus (control pattern) to shift in the present BSC. The *clockBscanAc* line is connected to the output of a flip-flop 512 that has two lines of input: *clockBscan* and *refClk*. Flip-flop 512 is generally common to all transmitting BSCs. Shift flip-flop 504 may comprise any generic D-type flip-flop. An output of shift flip-flop 504 is connected to an input of the update flip-flop 506. The output of shift flip-flop 504 is also connected to a *bscanShiftOut* line. The output of a flip-flop 514, having two lines of input: *updateBscan* and *refClk*, is also connected to the input of the update flip-flop 506. The shift flip-flop 504 may comprise any generic D-

BSC and the receiving BSC. And last, the reference clock is connected to the integrated circuits with this interface so that controls of skew are very easy. Thus, the BSCs as described above work as either ordinary IEEE 1149.1 or as AC JTAG cells.

[0055] While embodiments and applications of this invention have been shown and described, it would be apparent to those skilled in the art having the benefit of this disclosure that many more modifications than mentioned above are possible without departing from the inventive concepts herein. The invention, therefore, is not to be restricted except in the spirit of the appended claims. ← Correction 7

Serial/Patent.No.: 09/909,658 Filing/Issue Date: 7/19/01

Applicant: Chandrasekhar Thyamagondlu Srinivasaiah et al.

Title: Boundary Scan Cell For Testing AC Coupled Line Using Phase Modulation Technique

TRP Docket No.: CISCO-4330

Date Mailed: 6-17-04 Atty/Secty Initials: DBR/MA/cd

Docket Due Date: 6/17/04

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- ☐ Application – Rule 1.53(b) Continuation (_____ pgs.)
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- ☐ Certificate of Correction
- ☒ Certificate of Mailing
- ☐ Declaration & POA (_____ pgs.)
- ☒ Fee Transmittal
- ☒ Drawings (informal): Replacement Sheets- Figs. 1 & 2
  2 # of sheets includes 2 figures
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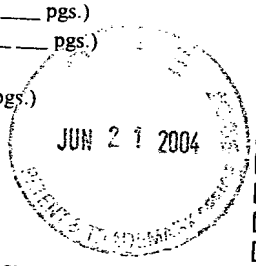

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- ☐ Check(s) $_____
- ☒ Deposit Acct. No. 50-1698 $$326.00
  Patent Code: 1201/1201/1251
  Client/Matter # 32590 - 158

AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [0048] with the following amended paragraph:

[0048] FIG. 7 is a flow diagram illustrating a method for enabling a transmitting Boundary Scan Cell (BSC) to operate with AC signals according to a specific embodiment of the present invention. In a first block 702, the transmitting BSC 502 detects whether it is functioning in AC JTAG mode. If the transmitting BSC 502 is not in AC JTAG mode, the reference clock input line *refclk* to the XOR logic gate 508 is held low in a block 704, thereby allowing the BSC to drive the same DC pattern as is present in the update register of the transmitting BSC. In block 706, if the transmitting BSC 502 is in AC JTAG mode, the transmitting BSC 502 is reset as described above. In block 708, the transmitting BSC generates AC signal based on the value of the transmitting BSC and the active reference clock as described above. The AC signal is then sent out to the receiving BSC 602 in block 710. Examples of AC signals produced by the transmitting BSC 602 are illustrated in FIG. 9A and 9B.

Correction 6

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings of claims in the application:

LISTING OF CLAIMS

1. (Currently Amended) A method for testing a circuit including AC coupled interconnects, the circuit ~~of a circuit~~ having a transmitting IC and a receiving IC that are coupled together by an AC interconnection, each IC having a Boundary Scan Cell (BSC) connected to a reference clock ~~and a source of an input signal~~, the method comprising:

generating an AC signal based on the reference clock and a value held in ~~of~~ the BSC of the transmitting IC ~~and the reference clock~~, the AC signal having a first phase if a first value is held in the BSC, and a second phase if a second value is held in the BSC;

generating, for the receiving IC, ~~transmitting~~ a sync pulse signal based on a test reset signal ~~to the BSC of the receiving IC;~~

capturing, in the BSC of the receiving IC, a default phase of said AC signal in response ~~relation~~ to said sync pulse signal;

sampling ~~capturing~~ a phase of the AC ~~input~~ signal;

comparing the default phase with the sampled ~~of the input signal with the~~ phase of the ~~said~~ AC signal ~~in relation to said sync pulse signal~~; and

generating a phase decode ~~sending an output~~ signal based on said comparing.

2. (Currently Amended) The method according to claim 1, wherein said generating an AC signal ~~further~~ comprises: ← Correction 8

resetting the BSC of the transmitting IC.

Correction 9

3. (Currently Amended) The method according to claim 2, wherein said resetting ~~further~~ comprises:

latching a default value ~~generating a zero value signal~~ in a boundary scan register in the BSC of the transmitting IC.

4-7. (Cancelled)

8. (Currently Amended) A system for testing a circuit including AC coupled interconnects, the circuit ~~of a circuit~~ having a transmitting ~~driving~~ IC and a receiving IC that are coupled together by an AC interconnection, each IC having a plurality of boundary scan cells (BSCs) connected to a reference clock, the system comprising:

means for generating an AC signal based on the reference clock and a value held in ~~of~~ the BSC of the transmitting IC ~~and the reference clock~~, the AC signal having a first phase if a first value is held in the BSC, and a second phase if a second value is held in the BSC;

means for generating ~~transmitting~~ a sync pulse signal based on a test reset signal ~~to the BSC of the receiving IC;~~

means for capturing, in the BSC of the receiving IC, a default phase of said AC signal in response ~~relation~~ to said sync pulse signal;

means for sampling ~~capturing~~ a phase of the AC ~~input~~ signal;

an XOR logic gate connected to said second flip-flop for generating an AC ~~the~~ signal based on a reference clock signal and the value held in said second flip-flop, the AC signal having a first phase if a first value is held in said second flip-flop, and having a second phase if a second value is held in said second flip-flop; and

a multiplexor for selectively outputting the AC signal based on a mode signal ~~sending the signal~~.

24. (Currently Amended) An input AC boundary scan cell (BSC), comprising:

a first flip-flop having a data input for receiving an input signal, a clock input connected to a *refClk* line, and a first flip-flop output, the input signal being an AC signal if said BSC is in an AC JTAG mode and a DC signal if said BSC is a non-AC JTAG mode, the first flip-flop output indicating a captured phase of the AC signal if the input signal is the AC signal;

a first multiplexer having a first input, a select input connected to a *syncPulse* ~~syncPulse~~ line, a second input connected to said first flip-flop output, and a first multiplexer output, a sync pulse signal on the *syncPulse* line having an initial pulse;

a second flip-flop having a data input connected to said first multiplexer output, a clock input connected to a *refClk* line, and a second flip-flop output feedback to said first input of said first multiplexer, said second flip-flop adapted to capture a default phase of the AC signal in the AC-JTAG mode when the sync pulse signal has the initial pulse, the second flip-flop output indicating the default phase;

Correction 10

an XOR logic gate having a first input connected to said second flip-flop output, a second input connected to said first flip-flop output, and an XOR logic gate output, the

Correction 11

XOR logic gate output having a first level if the first flip-flop output and the second flip-flop output match, and having a second level if the first flip-flop output and the second flip-flop output do not match;

a second multiplexer having a first input connected to said first flip-flop output, a select input connected to ~~and~~ an *acjtagMode* line, a second input connected to said XOR logic gate output, and a second multiplexer output;

a third multiplexer having a first input connected to a *bscanShiftIn* line, a select input connected to ~~and~~ a *ShiftBscan2Edge* line, a second input connected to said second multiplexer output, and a third multiplexer output; and

a third flip-flop having a first input connected to said third multiplexer output, a second input connected to a *clockBscan* line, and a third flip-flop output connected to a *bscanShiftOut* line.

25. (Currently Amended) An input AC coupled boundary scan cell (BSC) for receiving a signal, said BSC comprising:

a sampling flip-flop for sampling an input signal in accordance with ~~respect to~~ a reference clock, the input signal being an AC signal if said BSC is in an AC JTAG mode, the sampling flip-flop adapted to capture and output a phase of the AC signal if the input signal is the AC signal;

a feedback flip-flop connected to said sampling flip-flop, said feedback flip-flop adapted to capture a default phase of the AC signal when a sync pulse signal has an initial pulse, an output of said feedback flip-flop indicating the default phase ~~for controlling the signal~~; and

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